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ANALYSIS AND DESIGN OF HIGH CMRR INSTRUMENTATION AMPLIFIER FOR ECG SIGNAL ACQUISITION SYSTEM USING 180nm CMOS TECHNOLOGY

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ABSTRACT

This paper describes the design of Current Mode Instrumentation Amplifier (CMIA) for ECG signal Acquisition system. The CMIA topology is based on voltage mode operational amplifier (op-amp) power supply current sensing technique. Op amp mismatch and precise current mirrors are two design challenges of this topology. High Common Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio PSRR instrumentation amplifier is developed for biomedical applications. The proposed circuit uses a current mode structure to solve the conventional circuit's problems. The Simulation of proposed design is done on virtuoso 6.1.5 using UMC 0.18µm CMOS technology. Thus design achieves a very high CMRR 126dB up to 700 Hz and higher than 100dB up to 10KHz and PSRR 123 dB up to 616 Hz and higher than 100dB upto 10KHz, 39.68 dB closed loop gain and input referred noise is only 214 nV/sqrtHz @150 Hz at 1.8V single power supply

KEYWORDS: Analog Integrated Circuits, Bio Signal Amplifier, CMRR, Low Noise, Low-Power Circuit Design, PSRR

INTRODUCTION

Electrocardiogram (ECG), electroencephalogram (EEG) and electromyogram (EMG) are common bio-potential signals for clinic and health care applications. These signals have very low amplitudes and lie in very low frequency band [1] [4] as listed in Table 1.

Table 1: Bio-Potential Signals

Signal	Amplitude(µv)	Frequency(HZ)
ECG	1000-5000	0.5-150
EEG	10-50	0.1-100
EMG	50-5000	10-1000
EOG	10-100	DC-10

In order to extract the very weak, low frequency differential signals out from large common mode interference of human body, a well designed Instrumentation Amplifier (IA) is essential. The IA should have low input noise, low harmonic distortion, controllable voltage gain and high CMRR. Moreover, for long term and portable monitoring application, the IA is also required to have low power consumption and small size [1]. Hence, the circuit is expected to be implemented in a modern integrated circuit technology. CMRR is usually considered to be the most important parameter for instrumentation amplifiers.

In Voltage-Mode Instrumentation Amplifier (VMIA), CMRR is primarily limited by the mismatch of resistors rather than op-amps [3]. Laser trimming techniques have been employed to improve the resistor matching level in monolithic VMIA, providing CMRR magnitudes of as high as 90 dB. These techniques increase the cost of the device and are seldom used in current complementary metal -oxide–semiconductor processes.

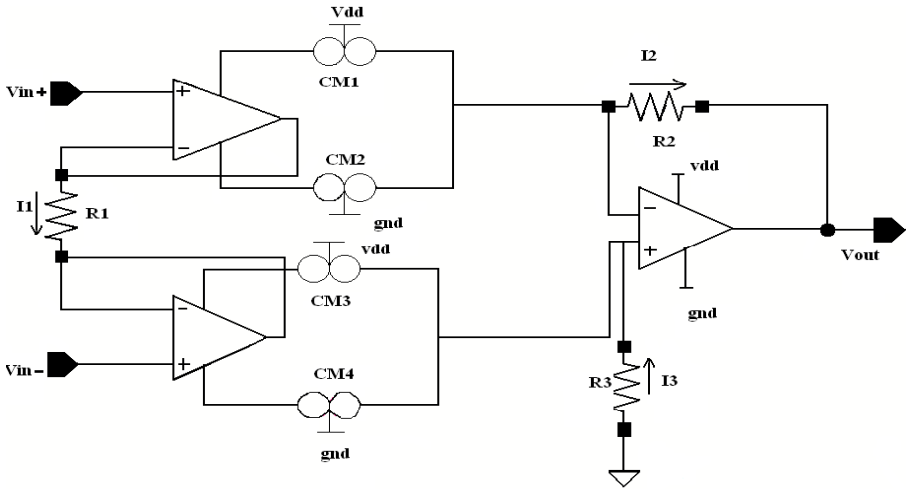

Figure 1: Proposed Current Mode Instrumentation Amplifier Topology

The CMIA is another technique that does not require highly accurate resistor matching to achieve a good CMRR. As a result of this design is more suited to a VLSI approach, leading to applications in implantable bio-medical devices [2] [5]. CMIA has several advantages compared with conventional instrumentation voltage mode amplifier, such as high CMRR which is affected by only a perfect matching of input op-amp (active block) which is independent of differential gain; voltage gain is independent of gain-bandwidth product and has no complex resistor mismatch.

This paper presents the design of CMIA in a CMOS 180nm technology. Theoretical analysis as well as circuit design with simulation results is presented using current mirrors as current summing network.

THEORETICAL ANALYSIS

Proposed Design

The schematic of the proposed CMIA topology is shown in Figure1 This CMIA consists of two input op-amps OP1 and OP2 and a resistor R1 as the differential input stage. Input stage is differential voltage to differential current converter stage. Output stage is a single ended current to voltage converter. Output stage converts current into a voltage using resistor R2. OP1 and OP2 are connected as unit gain buffers to convey the input voltages on resistor R1. Since a common mode voltage at the two terminals of R1 is expected to be equal to each other, only differential current I1 is flows through. Current I1 given by following equation (1)

$$I_1 = (V_{in+} - V_{in-})/R_1 \quad (1)$$

Where I1 is the output current of OP-1 and I2 is the output current of OP-2. Two current mirrors CM1 and CM2 are connected to both positive and negative power supply terminals of OP1 and copy a current (I2) as accurate as (I1) through R2, therefore, we get I1 = I2 = -I3. OP-3 and resistor R2 form the output stage of the CMIA. OP-3 is connected as transresistance amplifier to create a virtual ground at the outputs of CM1 and CM2 and convert I1 into voltage via R2. Once the differential current I1 flows through R2, a differential output voltage V_O is induced at the output terminal of OP-3. Differential output voltage V_O is given by equation (2)

$$V_o = I1\, R_2 \quad (2)$$

Putting value of I1 in equation (3)

$$V_o = (V_{in+} - V_{in-})\, R_2/R_1 \quad (3)$$

Hence, the overall differential gain is simply G_d = R2 / R1. Gain of instrumentation amplifier is adjusted by varying the value of R1 and R2. Ideally, common mode input voltage induces zero differential current; hence an infinity CMRR is obtained.

CMRR Analysis

The output stage of a CMIA is arranged as a buffer and cascaded to the input stage op amps, thus both its non idealities and its role in the total CMRR of the CMIA are minimized. Power supply voltage and current denoted as Vdd and I, respectively, it is also assumed that

$$\Delta Vdd = 0\,, \qquad I = I1 \tag{4}$$

Because of simple and more balanced circuitry, current mirrors have less effect on the total CMRR than the input op-amps. Consequently we can write output voltage (V_{O3}) of OP-3

$$V_{O3} = I_{O1}\,.R_2 = (V_{O1} - V_{O2})\frac{R_2}{R_1} \tag{5}$$

Where Io1(output current of OP- 1) = I1(input current of OP-3), V_{O1} is output voltage of OP-1, V_{O2} is output voltage of OP-2

$$V_{O1} = \left(V_{CM} - \frac{V_d}{2}\right)\frac{A_{OL1}}{1 + A_{OL1}} \tag{6}$$

$$V_{O2} = \left(V_{CM} - \frac{V_d}{2}\right)\frac{A_{OL2}}{1 + A_{OL2}} \tag{7}$$

where A_{OL1} is open loop gain of Op-1, A_{OL1} is open loop gain of Op-2, V_{CM} is common mode voltage and V_d is differential voltage

$$V_{O2} - V_{O1} = \left[\left(V_{CM} + \frac{V_d}{2}\right)\frac{A_{OL2}}{1 + A_{OL2}}\right] - \left[\left(V_{CM} - \frac{V_d}{2}\right)\frac{A_{OL1}}{1 + A_{OL1}}\right] \tag{8}$$

If $V_d = 0$

$$V_{O2} - V_{O1} \approx V_{CM}\left(\frac{A_{OL2} - A_{OL1}}{A_{OL1}A_{Ol2}}\right) \tag{9}$$

$$A_{CM} = \frac{V_{O2} - V_{O1}}{V_{CM}} \approx \left(\frac{A_{OL2} - A_{OL1}}{A_{OL1}A_{Ol2}}\right) \tag{10}$$

CMRR in dB = 20 log $\left|\frac{\text{Difrential Voltage Gain}}{\text{Comman Mode Voltage Gain}}\right|$ = 20 log $\left|\frac{A_d}{A_{CM}}\right|$

$$CMRR \propto \left|\frac{A_{OL2}A_{OL1}}{A_{OL2} - A_{OL1}}\right| \tag{11}$$

From (8), high CMRR requires either high differential gains or matched differential mode and common mode gains of input op-amps [9]. Since high gain op-amp is not practical for modern CMOS technology and according to

equation (11) well matched differential mode gains and CMRRs of OP-1 and OP-2 are dominative to the overall gain and easier to be adjusted than common mode gain. It is advisable to possibly make CMRRs of input op-amps matched but not the common mode gain.

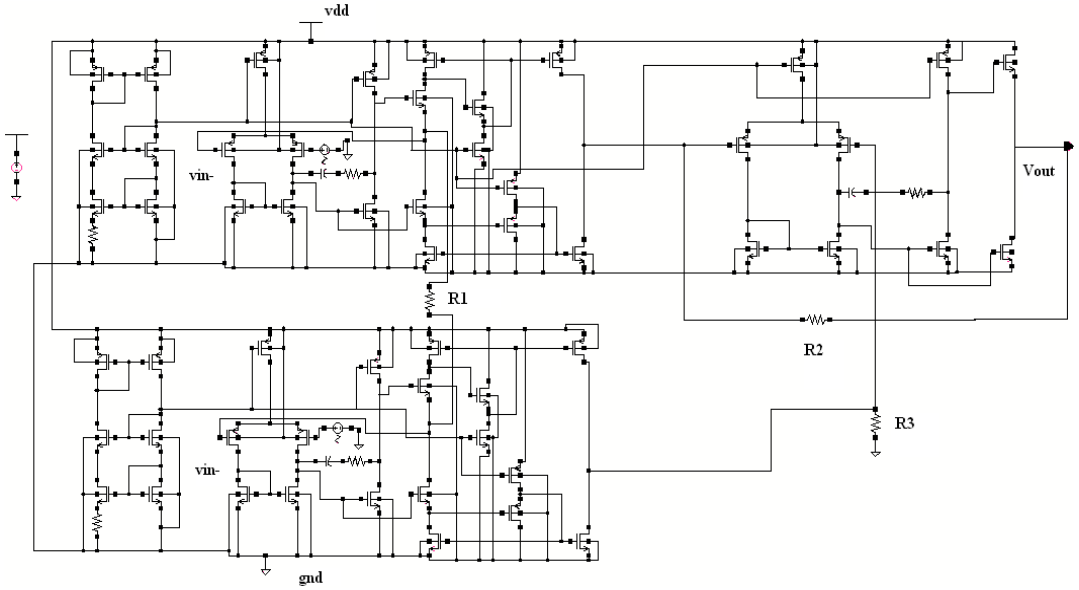

Figure 2: Complete MOS Level Schematic of Proposed CMIA

BASIC BUILDING BLOCKS IMPLEMENTATION

Operational Amplifier (Op-Amp)

The schematic of op amp is designed from three-stage topology with miller-compensated capacitor. In Figure 3 transistors M1-M7 op-amp. The current mirrors CM1, CM2, CM3 and CM4 are built on the output stages of them.

Flicker noise is caused mainly due to the interface trap Density in NMOS and mobility fluctuations in PMOS. It is a major concern when designing low frequency circuitry PMOS is the preferred choice for the input transistors as flicker noise is found at least one order lower than that of NMOS [6] [8].

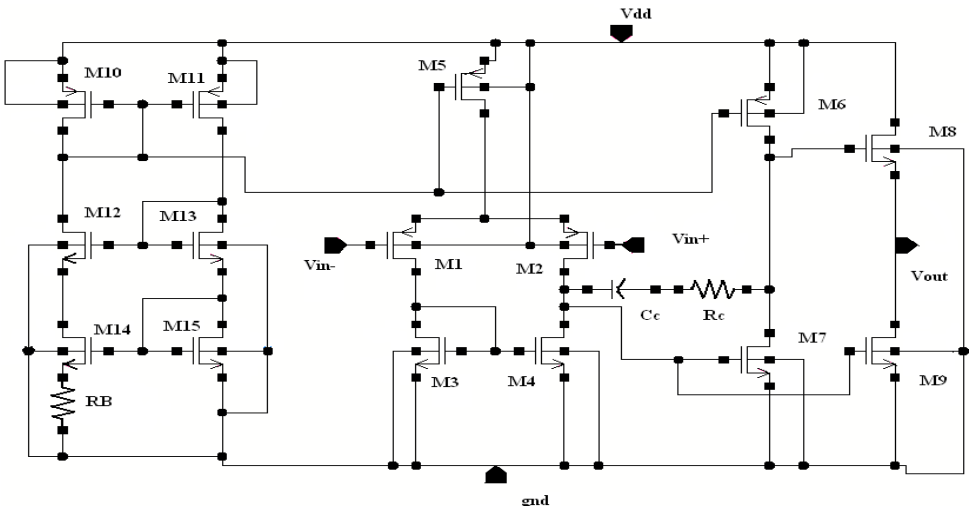

Figure 3: MOS Level Schematic of Three Stage Op-Amp

It is important to note that the output impedance should be designed carefully. Mismatch of this parameter also decreases the CMRR performance of the CMIA. Figure 3 has three stages, two gain stages and a unity gain output stage. The output buffer stage is normally present only resistive loads which need to be driven Table 2 shows the simulated result of input op-amps and Figure 4 is the simulated frequency response.

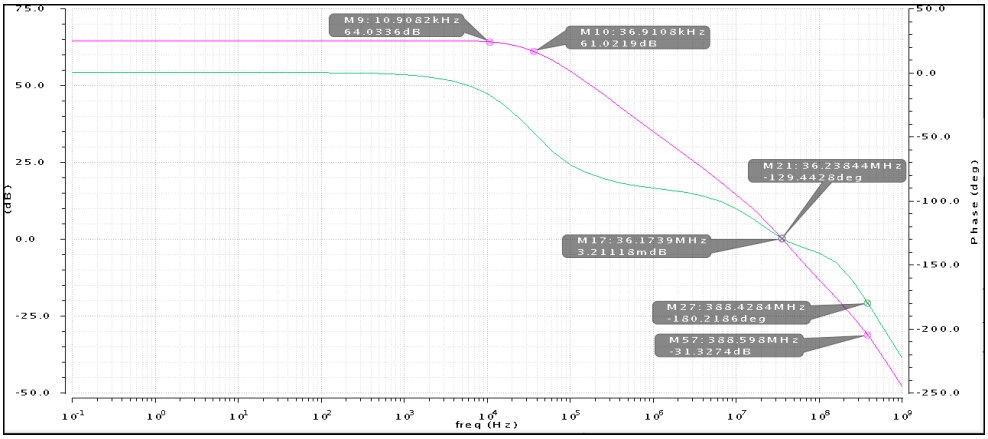

Figure 4: Frequency Response of Input Op-Amp

Current Mirror

Mismatch of input op-amps is a serious problem of CMRR performance, but current mirrors also play significant role [2] [5]. In 180nm technology has transistors have threshold voltages of approximately ± 500mV. It means that a standard n channel or p channel current mirror will require an output voltage more than +600mV to remain in the active mode of operation [7] [10]. In this work two current mirrors are required at each input op-amp, leaving only 600mV for op-amp operation.

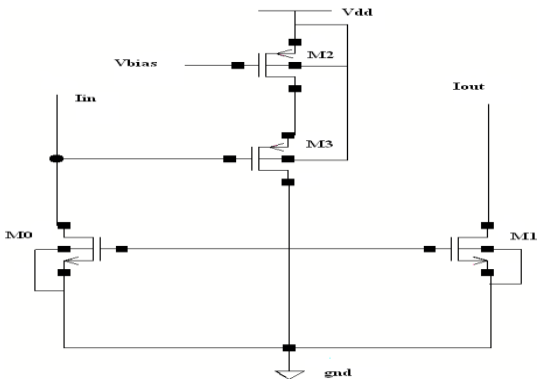

Figure 5: MOS Level Schematic of Current Mirror

In Figure 5 low-voltage standard N channel current mirror with a level-shifter between the gate and drain of the input transistor is shown. The principle behind this topology is that the gates of the devices are not directly connected to the input of the mirror. Instead, there is additional circuitry that "shifts" the voltage level. This allows the input of the mirror and the gates of the mirroring devices to have different voltages. Thus, the gates of the mirroring devices can be biased at a relatively high voltage while the input and output voltages can remain relatively low. The voltage gain, Av, of this circuit is

$$A_v \approx \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} \quad (10)$$

In this work level shifter is implemented using a source follower stage. This allows the current mirror to operate with an output voltage requirement equivalent to approximately 100mV~200mV.

SIMULATION RESULTS

The instrumentation amplifier is designed with the CMOS 0.18 µm technology. Figure 4 shows the open-loop gain of input op-amp1 (op-amp2) which is 64dB.The simulations are performed with Spectre in analog environment.

Figure 6 shows the frequency response of instrumentation amplifier which has close loop gain close to 39.6 dB and the unity gain bandwidth is around 6.6MHz. Figure 7 shows variation in gain with feedback resistance which is increases with high value of feedback resistance. The CMIA keeps a CMRR (Figure 8) 126dB up to700 Hz and higher than 100dB up to 10k Hz which satisfies the basic standard of medical instruments. Figure 9 shows CMIA with PSRR 123 dB up to 616 Hz and higher than 100dB up to 10k Hz. Figure 10 shows the noise performance which shows 214 nV/sqrt Hz @ 150 H, for those applications concerning the signal band lower than 0.1 Hz, the chopping technique is required to further reduce the noise within this frequency band. Settling time of CMIA is150 ns, positive and negative slew rate is nearly equal which is +1.62 Volts/µsec, - 1.76 Volts/µsec respectively. Table 3 gives a summary of the simulation results.

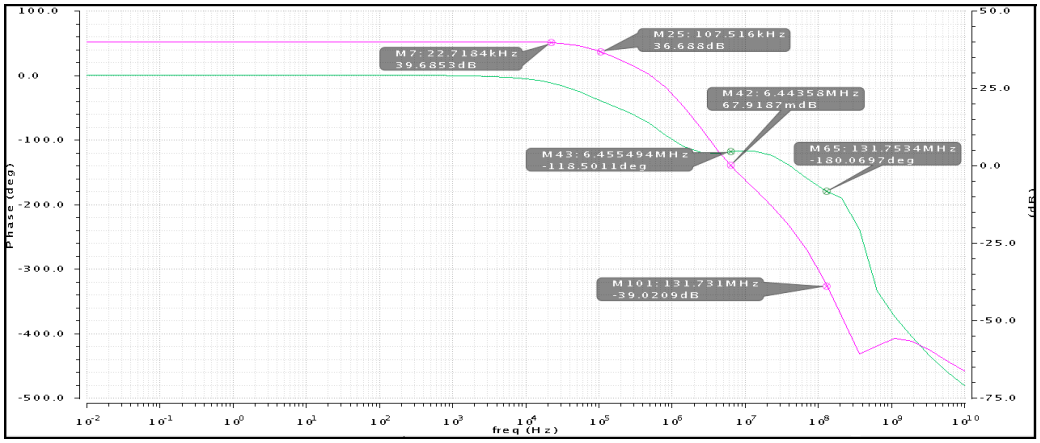

Figure 6: Frequency Response of CMIA

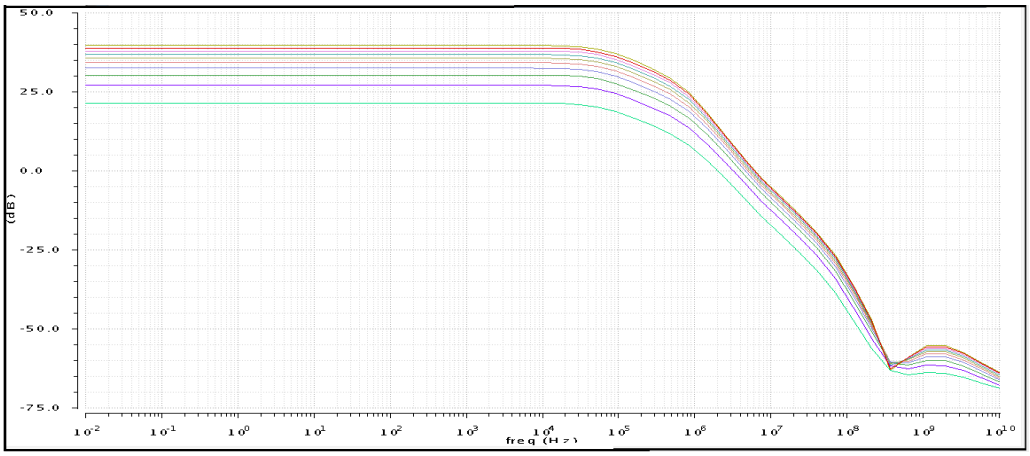

Figure 7: Effect of Feedback Resistance on Gain

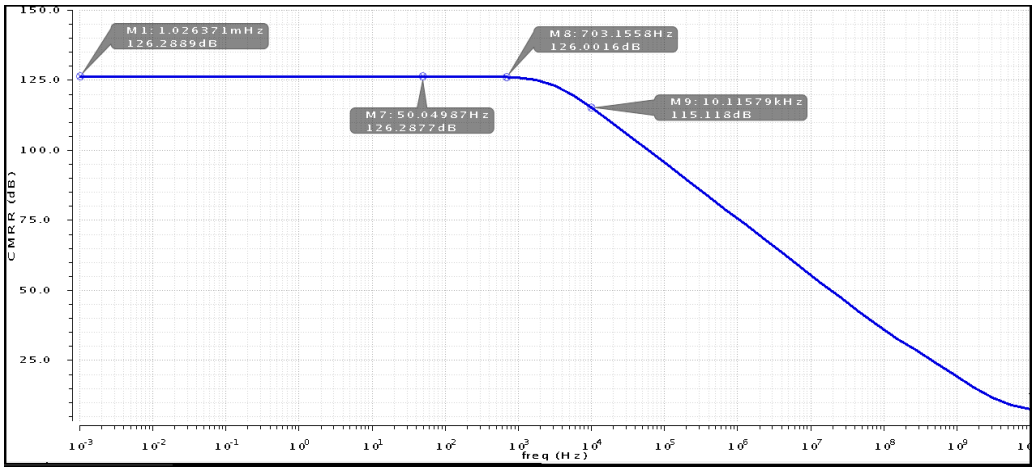

Figure 8: CMRR Plot of CMIA

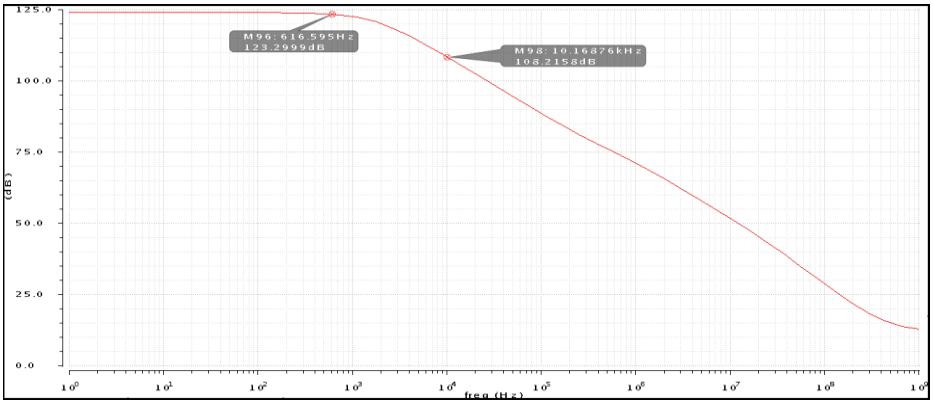

Figure 9: PSRR Plot of CMIA

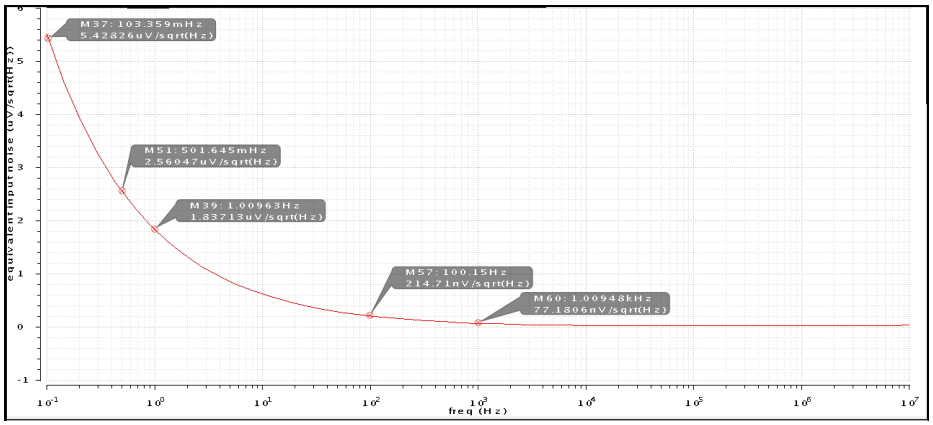

Figure 10: Equivalent Input Noise Response of CMIA

Table 2: Simulated Results of Op-Amp

Specification	Simulated Results
Gain	39.6dB
Phase Margin(PM)	49˚
-3dB Frequency	100K
Gain Margin (GM)	39dB
Gain Bandwidth	6.44MHz
CMRR	126 dB
PSRR	123 dB
Input Referred Noise	214nV/sqrt Hz@ 150
Equivalent output noise	23uV/sqrt Hz@ 150 Hz
Power Consumption	1.24mW
Positive Slew Rate	+1.622Volts/µsec
Negative Slew Rate	−1.76Volts/µsec
Settling Time	150ns

Table 3: Simulated Results of CMIA

Specification	Simulated Result
Open loop Gain	64 dB
Phase Margin(PM)	51˚
-3dB Frequency	36K
Gain Margin (GM)	31dB
Unity Gain Bandwidth	36MHz
CMRR	94dB (0.1 Hz to 10KHz)
PSRR	110 dB up to 1KHz
Input Referred Noise(rms)	550n/sqrt Hz@ 150 Hz
Equivalent output noise	416uV/sqrt Hz@ 150 Hz
Power Consumption	182 µW

CONCLUSIONS

A current mode instrumentation amplifier using op amp power supply current sensing technique for bio-signal acquisition system is implemented and analyzed in a CMOS 0.18μm technology. The proposed circuits combine current mirrors that can deal with the problem of resistors matching as in the conventional instrumentation amplifier circuits. Simulation results show that the CMIA demonstrates continuous GBW-independent gain adjustment function and good signal distortion performance. The circuit has 126 dB CMRR up to 700 Hz and keeps a value higher than 100 dB up to 10KHz and equivalent input noise voltage is 77nV/$\sqrt{HZ}$ at 1KHz. Chopping technique is required to further reduce input noise voltage frequency lower than 0.1 Hz. The CMIA consumes only 1.24mW at 1.8 V dc supply voltage which is suitable for bio-signal application. Power can be reduced further by operating transistor in sub threshold region. The circuit does not require advanced op-amp design but the matching between op-amps plays an important role in layout phase. The accurate current mirror is the main challenge in schematic phase for higher CMRR and better signal quality.

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